

dicating the capacitance between the wrench socket and the bolt head.

The algorithm processing the digitized capaciflector readings would exploit the fact that for any fixed position of the wrench socket along the central axis of the bolt head, the capacitance would reach a minimum when the axis of the wrench socket coincided with the axis of the bolt head and the wrench socket was clocked (rotated about its axis) to the angular position

for mating with the bolt head: any lateral (horizontal in the figure) translation or any rotation of the wrench socket away from the central position and the mating orientation would cause an increase in capacitance. Hence, for a given fixed position along the center line of the bolt, the information needed to correct any deviation of the wrench socket from the central position and the mating orientation could be obtained by taking capaci-

tance measurements during a sequence of controlled dithers of the position and orientation along and about the various coordinate axes. This is analogous to the feel a skilled craftsman instinctively uses, except it is non-contact, hence, "virtual feel."

*This work was done by John M. Vranish of Goddard Space Flight Center. Further information is contained in a TSP (see page 1).
GSC-14955-1*

FETs Based on Doped Polyaniline/Polyethylene Oxide Fibers

Advantages include tailorability of electronic properties and low power demands.

John H. Glenn Research Center, Cleveland, Ohio

A family of experimental highly miniaturized field-effect transistors (FETs) is based on exploitation of the electrical properties of nanofibers of polyaniline/polyethylene oxide (PANi/PEO) doped with camphorsulfonic acid. These polymer-based FETs have the potential for becoming building blocks of relatively inexpensive, low-voltage, high-speed logic circuits that could supplant complementary metal oxide/semiconductor (CMOS) logic circuits.

The development of these polymer-based FETs offers advantages over the competing development of FETs based on carbon nanotubes. Whereas it is difficult to control the molecular structures and, hence, the electrical properties of carbon nanotubes, it is easy to tailor the electrical properties of these polymer-based FETs, throughout the range from insulating through semiconducting to metallic, through choices of doping levels and chemical manipulation of polymer side chains. A further advantage of doped PANi/PEO nanofibers is that they can be made to draw very small currents and operate at low voltage levels, and thus are promising for applications in which there are requirements to use many FETs to obtain large computational capabilities while minimizing power demands.

Fabrication of an experimental FET in this family begins with the preparation of a substrate as follows: A layer of silicon dioxide between 50 and 200 nm thick is deposited on a highly doped (resistivity $\approx 0.01 \Omega\cdot\text{cm}$) silicon substrate, then gold electrodes/contact stripes are deposited on the oxide. Next, one or more fibers of camphorsulphonic acid-doped PANi/PEO having diameters of the order of 100 nm are electrospun onto the sub-

strate so as to span the gap between the gold electrodes (see Figure 1).

Figure 2 depicts measured current-versus-voltage characteristics of the device of Figure 1, showing that saturation channel currents occur at source-to-

drain potentials that are surprisingly low, relative to those of CMOS FETs. The hole mobility in the depletion regime in this transistor was found to be $1.4 \times 10^{-4} \text{ cm}^2/(\text{V}\cdot\text{s})$, while the one-dimensional charge density at zero gate bias was esti-

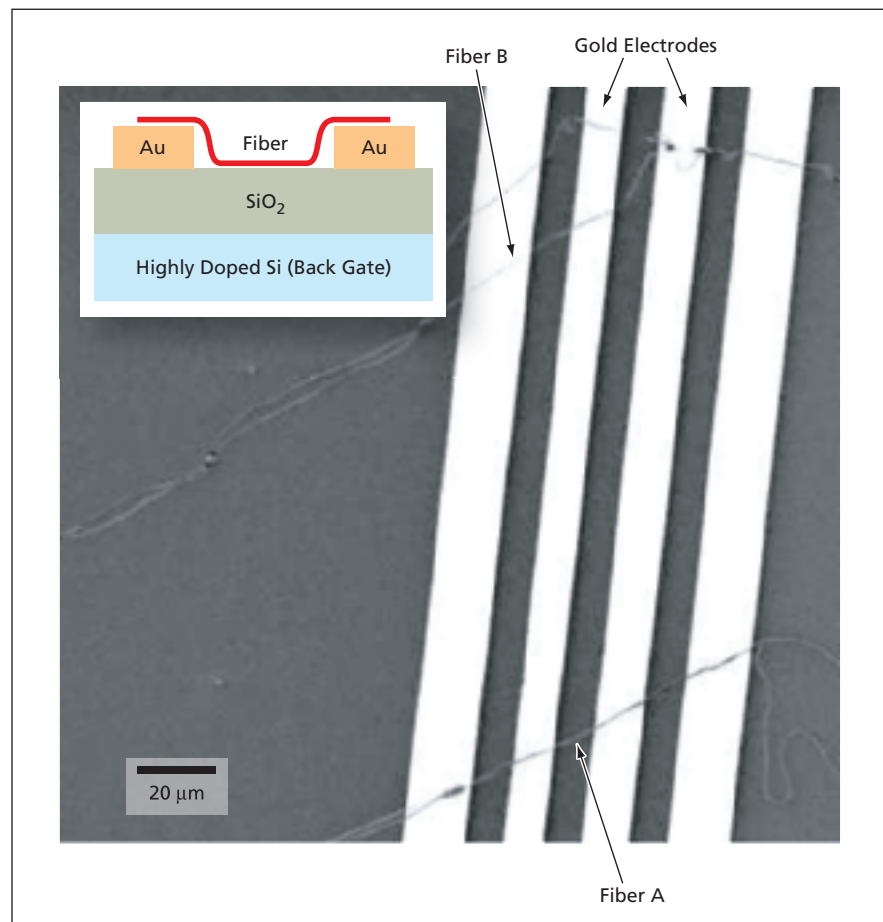


Figure 1. Fibers of Doped PANi/PEO are electrospun across the gap between source and drain gold electrodes on a prepared substrate to form an FET. The inset presents a simplified cross section showing one fiber. The rest of the picture is a scanning electron micrograph, wherein fiber A (12 μm long, 300 nm in diameter) and fiber B (18 μm long, 120 nm in diameter) in contact with the two inner gold electrodes are parts of an experimental FET.

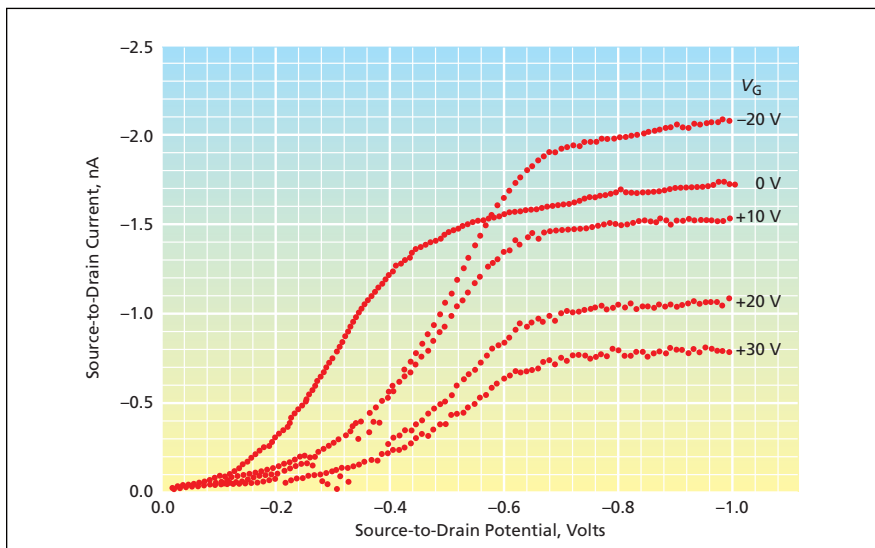


Figure 2. These **Current-Versus-Voltage Characteristics** were obtained from measurements on the FET of Figure 1. The measurements were made at various values of back gate voltage (V_G) representative of the accumulation and depletion modes.

mated to be approximately one hole per 50 two-ring repeat units of polyaniline, consistent with the rather high channel conductivity ($\approx 10^{-3}$ S/cm). Reducing or eliminating the PEO content of the fibers is expected to enhance the properties of future versions of this transistor.

*This work was done by Noulie Theofylaktos, Daryl Robinson, and Félix Miranda of **Glenn Research Center**; Nicholas Pinto of the University of Puerto Rico; Alan Johnson, Jr. and Alan MacDiarmid of the University of Pennsylvania; and Carl Mueller of Analox Corp. Further information is contained in a TSP (see page 1).*

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-17933-1.

Miniature Housings for Electronics With Standard Interfaces

Marshall Space Flight Center, Alabama

A family of general-purpose miniature housings has been designed to contain diverse sensors, actuators, and drive circuits plus associated digital electronic readout and control circuits. Each housing fits within an envelope having dimensions of about $2\frac{1}{4}$ by $1\frac{3}{4}$ by $\frac{1}{2}$ in. (about 5.7 by 4.4 by 1.3 cm). Each housing can be secured to a mating carrier by use of screws or epoxy; this mounting scheme helps the housings and their contents to withstand severe vibrations and ensures thermal conduction for dissipation of heat generated during operation of the

contained circuitry. The circuits contained in the housings communicate with the external world via standard RS-485 interfaces. Multiple units comprising housings and their contents can easily be electrically connected together in a daisy-chain arrangement, within which individual units are addressable via the RS-485 bus. Hence, a single master computer connected to the bus can program, or read data from, any or all such units. Examples of such units include small motor drives, programmable thermostats, data loggers, and programmable

controllers. There are numerous potential uses for these units in medical equipment, automotive electronics, manufacturing equipment, and robots.

*This work was done by David E. Howard, Dennis A. Smith, and Dean C. Alhorn of **Marshall Space Flight Center**. Further information is contained in a TSP (see page 1).*

This invention is owned by NASA, and a patent application has been filed. For further information, contact Sammy Nabors, MSFC Commercialization Assistance Lead, at sammy.a.nabors@nasa.gov. Refer to MFS-32000-1.